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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,438	06/24/2003	Nicholas Shaylor	SUN03-0097	4376
57960	7590	11/28/2006	EXAMINER	
SUN MICROSYSTEMS INC. C/O PARK, VAUGHAN & FLEMING LLP 2820 FIFTH STREET DAVIS, CA 95618-7759			RUTTEN, JAMES D	
			ART UNIT	PAPER NUMBER
			2192	

DATE MAILED: 11/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/603,438

Applicant(s)

SHAYLOR ET AL.

Examiner

J. Derek Rutten

Art Unit

2192

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 June 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

1. Claims 1-21 have been examined.

#### ***Specification***

2. The disclosure is objected to because of the following informalities: The reference to a copending application is listed in paragraph [0002] and appearing on page 2 of the specification with serial number and filing date "TO BE ASSIGNED," which should be updated with the proper numbers and dates.

Appropriate correction is required.

#### ***Claim Objections***

3. Claims 4, 11, and 18 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claims, or amend the claims to place the claims in proper dependent form, or rewrite the claims in independent form. For example, the "parameters" of claim 4 are interpreted as being equivalent to the "operands" of claim 1, and therefore has no limiting effect on the claim. The same language is found in claims 8/11 and 15/18.

#### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1, 2, 4-9, and 11-14 are rejected under 35 U.S.C. 102(a) as being anticipated by “Bytecode verification on Java smart cards” by Leroy (hereinafter “Leroy”).

In regard to claim 1, Leroy discloses:

*A method to facilitate code verification and garbage collection in a platform-independent virtual machine* See sections 4.1 and 4.2 for a description of methods for “stack normalization” and “register reallocation”. Note that these methods facilitate verification and garbage collection at least according to Leroy’s Summary on page 319 (e.g. “simplify the bytecode verifier”), as well as the description of register reallocation in light of the discussion of garbage collection difficulties as appearing in paragraph [0008] in the “Related Art” section on page 3, lines 22-25, of Applicants’ specification.

*receiving a code module written in a platform-independent language;* See page 319, paragraph 3 in section 1, e.g. “Java”.

*examining the code module to locate a call to a program method within the code module;* See page 321, 2<sup>nd</sup> paragraph in section 2, “each non-abstract method”.

*transforming the code module so that all operands remaining on an evaluation stack when the program method is called relate to the program method.* See page 325, e.g. “Requirement R1. The operand **stack is empty** at all branch instructions (after popping the **branch arguments**, if any)...” [emphasis added]. Note that branch arguments are directly related to the branch, or method. Also see page 329, section 4: “Off-Card Code Transformations.”

Note that the “whereby” clause “*whereby verification and garbage collection of the code module is simplified*” appears to be expressing an intended result of the method that does not require the steps to be performed. Therefore, this clause has not been given weight. See MPEP 2111.04.

In regard to claim 2, the above rejection of claim 1 is incorporated. Leroy further discloses: *wherein transforming the code module involves ensuring that local variables hold only values of a single type and do not hold variables of different types at different times*. See section 4.2 “Register reallocation” on pages 333-335.

In regard to claim 4, the above rejection of claim 1 is incorporated. All further limitations have been addressed in the above rejection of claim 1. Note that the claimed “parameters” are interpreted as equivalent to the “operands” of claim 1.

In regard to claim 5, the above rejection of claim 1 is incorporated. Leroy further discloses: *wherein transforming the code module further comprises spilling to memory stack slots that do not include operands for the call to the program method*. See section 4.1 “Stack normalization” on pages 329-333.

In regard to claim 6, the above rejection of claim 5 is incorporated. Leroy further discloses: *filling stack slots that were previously spilled upon return from the program method*. See page 329, section 4.1, e.g. “loads.”

In regard to claim 7, the above rejection of claim 6 is incorporated. Leroy further discloses: *wherein the program method is associated with a single typemap to indicate a type for each variable on the evaluation stack*. See page 323, 2<sup>nd</sup> paragraph in section

2.3, e.g. “[a] method ... leading to a dictionary”. Leroy’s dictionary associates stack and register types. See page 322, 2<sup>nd</sup> paragraph in section 2.2.

In regard to claim 8, Leroy discloses an apparatus. See section 5.2, e.g. “500 MHz Pentium III.” All further limitations have been addressed in the above rejection of claim 1.

In regard to claims 9 and 11-14, the above rejection of claim 8 is incorporated. All further limitations have been addressed in the above rejection of claims 2 and 4-7, respectively.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leroy in view of “Garbage Collection and Local Variable Type-Precision and Liveness in Java™ Virtual Machines” by Agesen et al. (hereinafter “Agesen”).

In regard to claim 3, the above rejection of claim 1 is incorporated. Leroy discloses removing operands at branch instructions (see page 325, “Requirement R1”).

Leroy does not expressly disclose: *wherein transforming the code module involves*

*ensuring that the evaluation stack includes only elements related to a bytecode that may trigger garbage collection when the bytecode is executed.* However, Agesen discusses garbage collection points, i.e. “gc points,” as including calls, and loops that correlate with branches. See page 271 middle of column 2. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Agesen’s gc points with Leroy’s operand requirements in order to simplify the reclamation of memory (see Agesen page 269 1<sup>st</sup> paragraph on section 1).

In regard to claim 10, the above rejection of claim 8 is incorporated. All further limitations have been addressed in the above rejection of claim 3.

8. Claims 15, 16, and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leroy in view of US Patent No. 6,047,125 to Agesen et al. (hereinafter “the ’125 patent”).

In regard to claim 15, Leroy discloses:

*A computer system (see 3<sup>rd</sup> paragraph of section 5.2, e.g. “PC”) to facilitate code verification and garbage collection in a platform-independent virtual machine, comprising:*

*a central processing unit; see 3<sup>rd</sup> paragraph of section 5.2, e.g. “Pentium III” and a receiving mechanism within the central processing unit configured to receive a code module written in a platform-independent language; Note that any system that runs code must contain this feature, otherwise code would be unable to be loaded in order to execute.*

Leroy does not expressly disclose: *a memory system; a port for communicating with an external client; or a bus to couple the central processing unit, the memory system, and the port*; However, Agesen teaches:

*a memory system*; E.g. "System RAM" element 110 FIG. 3A

*a port for communicating with an external client*; E.g. "Communication Adapter" element 190 FIG. 3A

*a bus to couple the central processing unit, the memory system, and the port*; E.g. "Bus" element 130 FIG. 3A

All further limitations have been addressed in the above rejection of claim 1.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the components of the '125 patent with Leroy's system in order to implement garbage collection methods (see the '125 patent column 7 lines 24-25).

In regard to claims 16 and 18-21, All further limitations have been addressed in the above rejection of claims 2 and 4-7, respectively.

9. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leroy in view of the '125 patent, and further in view of Agesen.

In regard to claim 17, the above rejection of claim 15 incorporated. All further limitations have been addressed in the above rejection of claim 3.




***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. Derek Rutten whose telephone number is (571)272-3703. The examiner can normally be reached on T-F 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571)272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JDR

  
TUAN DAM  
SUPERVISORY PATENT EXAMINER